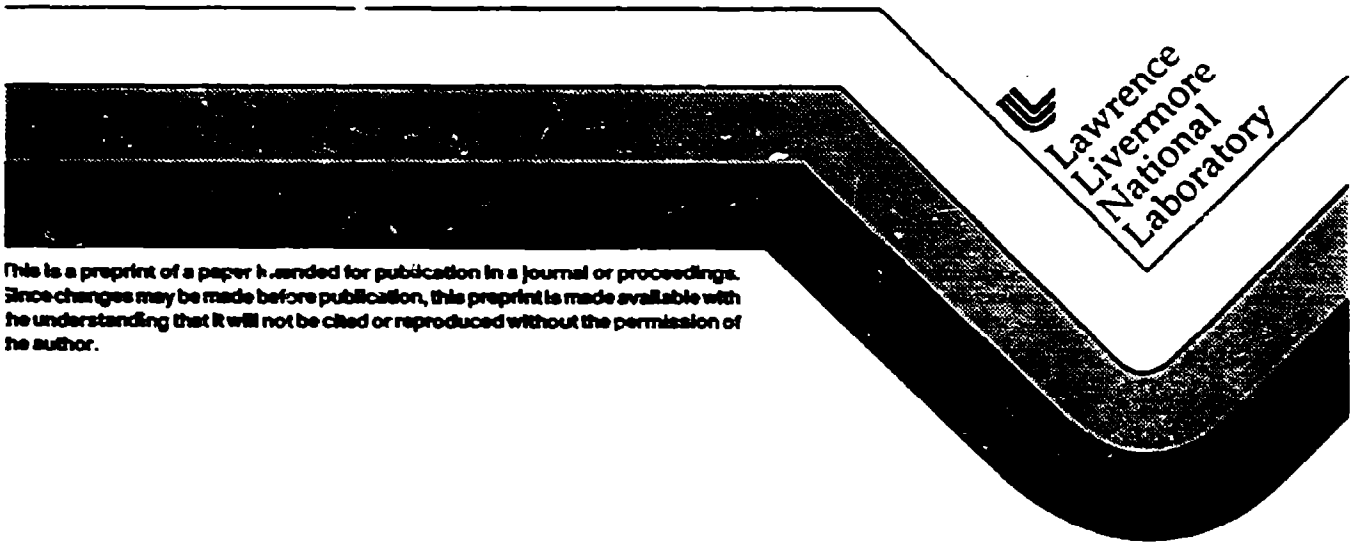
UCRL-JC-113618
PREPRINT

Electrochemical Planarization for Microelectronic Circuits

Robert J. Contolini
Steven T. Mayer
Anthony F. Bernhardt

This paper was prepared for distribution at
the NCAICM Workshop
(National Center for Advanced Information Components Manufacturing)
Albuquerque, New Mexico
March 30-31, 1993

March 25, 1993



Lawrence Livermore National Laboratory
University of California

ELECTROCHEMICAL PLANARIZATION FOR MICROELECTRONIC CIRCUITS

A Significantly Improved Process

Need for Flatter Surfaces

The need for flatter and smoother surfaces (planarization) in microelectronic circuits increases as the number of metal levels in ultra large scale integrated (ULSI) circuits increases. The flatter—or more planarized—each layer of material is, the more layers that can be made. More layers yield a denser circuit wiring, a higher final product computation speed, and a less expensive final product, due to a lower number of defects.

Electrochemically Flatter Is Easier and Less Expensive

We have developed an electrochemical planarization process. It first involves the uniform blanket metal electroplating over an insulating layer having embedded conductor lines. The next step is to remove the metal very uniformly, leaving behind embedded conductors that have their top surfaces level with the top surfaces of the surrounding insulator layer. This step has conventionally been carried out by a process called chemical-mechanical polishing (CMP). In CMP, the excess electroplated metal, along with the insulating material, is mechanically polished away (aided by simultaneous chemical etching) until the embedded conductors remain.

At LLNL, we have developed a significantly improved process and apparatus using electropolishing to smoothen and remove the metal layer very uniformly across the surface of the sample. A sample coated with copper is placed in a viscous acid bath, rotated, and an electric current is applied between the sample (positive connection) and the counter electrode (negative connection). Copper is removed from the surface of the sample in an "electropolishing mode," which smoothens the surface. The polishing results from a microscopic preferential removal of metal from more exposed areas. On a macroscopic basis, the material is removed uniformly. When finished, the surface copper becomes mirror smooth.

Applications

- *Planarization of electronic circuits at ULSI level*
- *Planarization of electronic circuits at the packaging level*
- *Uniform metal thinning and planarization on other substrates such as optical components (mirrors, thin windows), metal samples for scanning electron or scanning transmission electron microscopy*
- *Uniform, selective removal of coatings on semiconductors or other substrates.*
- *Low-cost optical mirrors on nonsmooth substrates*

Our Process Details

We have developed an electrochemical planarization process that fills vias and trenches with metal (without voids) and subsequently planarizes the surface. We make use of plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 for the dielectric layers (although polyimide also works satisfactorily) and electroplated copper for the metalization. Our electroplating tools produce low-resistance (<1.9 μohm-cm) conductors and are low in cost and maintenance compared to vacuum metalization equipment. Blanket electroplating completely fills the trenches and vias and partially planarizes the surface. Electropolishing further planarizes the surface down to a thin (1000-5000 Å) metal layer. Finally, either an ion-milling or a wet-etch process removes the remaining metal. The process can be repeated as necessary for multilevel metallization.

Advantages Over Existing Products

- More accurate endpoint determination
  a) Visually by eye
  b) By measuring the amount of charge passed through the sample
  c) Colorimetrically by detector

Lawrence Livermore National Laboratory
University of California

- Easily adaptable to robotic handling
- Easily adaptable to assembly line type manufacturing
- Better uniformity of metal polishing removal
- Virtually infinite selectivity of metal over insulator removal
- Less expensive capital costs
- Electropolisher machine weight is about one-eighth of conventional polishing machines

Open for Collaboration

The Laboratory is seeking an organization interested in collaborating on further improvements for this and related technologies.

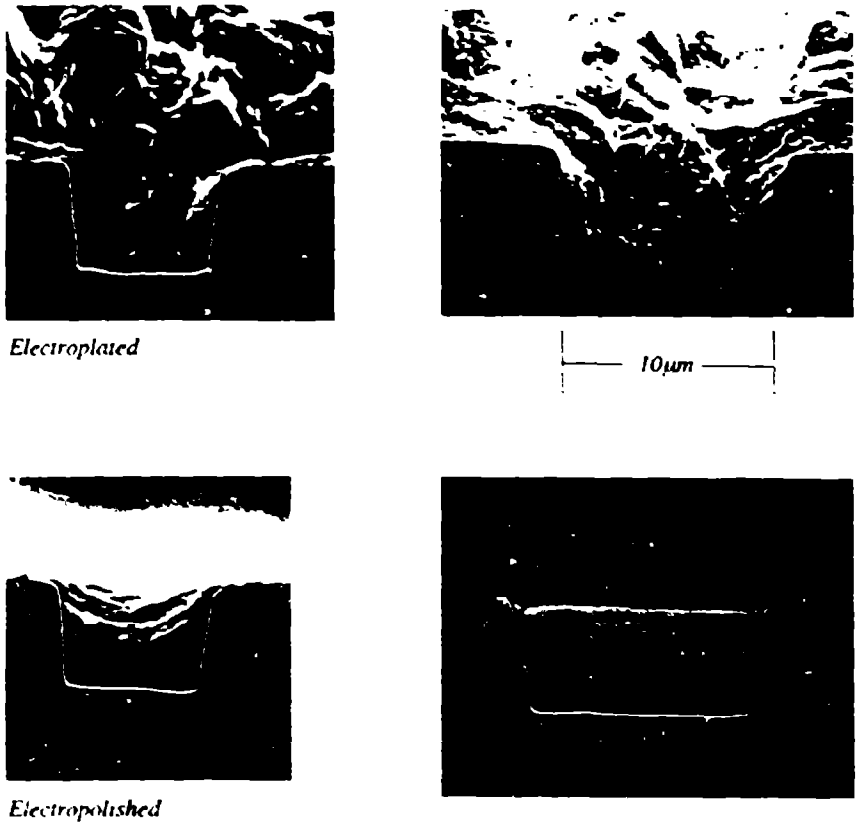
Previous Technology Transfer

We transferred our electropolishing technology and a new machine to IBM, which is investigating the use of the machine and electropolishing process for planarization. Transferring this technology to industry earned us the prestigious 1992 Excellence in Technology Transfer Award from the Federal Laboratory Consortium, which recognizes distinguished work of sigificant value to U.S. industries.

For More Information:

Contact: *Robert Contolini/Tony Bernhardt*
Tel. No *(510) 462-1225/(510)-423-7801*
Fax: *(510) 422-7309*
Mail Code *L-271/L-322*

Technology Transfer Initiative Program
Lawrence Livermore National Laboratory
7000 East Avenue, Mail Stop L-795
Tel. No: (510) 422-6416
Fax No: (510) 423-8988



Planarization of different width conductors

Acknowledgement: This work was performed under the auspices of the U.S. DOE by LLNL under contract no. W-7405-Eng-48.